

**METHOD OF REDUCING DISLOCATION-INDUCED
LEAKAGE IN A STRAINED-LAYER FIELD-EFFECT TRANSISTOR**

ABSTRACT OF THE DISCLOSURE

[0027] A structure and method of fabricating a semiconductor field-effect transistor (MOSFET) such as a strained Si n-MOSFET where dislocation or crystal defects spanning from source to drain is partially occupied by heavy p-type dopants. Preferably, the strained-layer n-MOSFET includes a Si, SiGe or SiGeC multi-layer structure having, in the region between source and drain, impurity atoms that preferentially occupy the dislocation sites so as to prevent shorting of source and drain via dopant diffusion along the dislocation. Advantageously, devices formed as a result of the invention are immune to dislocation-related failures, and therefore are more robust to processing and material variations. The invention thus relaxes the requirement for reducing the threading dislocation density in SiGe buffers, since the devices will be operable despite the presence of a finite number of dislocations.